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CAPACITOR FABRICATION METHODS AND CAPACITOR CONSTRUCTIONS

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CAPACITOR FABRICATION METHODS AND CAPACITOR CONSTRUCTIONS

TECHNICAL FIELD

The aspects of the invention relate to capacitor fabrication methods including forming insulative barrier layers and capacitor constructions having insulative barrier layers.

BACKGROUND OF THE INVENTION

Capacitors are common devices used in electronics, such as integrated circuits, and particularly semiconductor-based technologies. Two common capacitor structures include metal-insulator-metal (MIM) capacitors and metal-insulator-semiconductor (MIS) capacitors. One important factor to consider when selecting a capacitor structure may be the capacitance per unit area. MIS capacitors may be advantageous since a first electrode as the semiconductor may be formed of hemispherical grain (HSG) polysilicon that exhibits a higher surface area in a given region compared to a planar surface of amorphous polysilicon. The higher surface area provides more capacitance per unit area occupied by a capacitor.

However, a high K factor (also known as dielectric constant or "κ") dielectric material may be desirable to further enhance capacitance. Ta₂O₅ is one example of a high K factor dielectric, but it inherently forms an interfacial dielectric layer of SiO₂ when formed on a capacitor

1 electrode comprising HSG. The interfacial dielectric exhibits a lower K
2 factor than Ta_2O_5 , and thus reduces the effective dielectric constant for
3 the capacitor construction. Such reduction may be significant enough to
4 eliminate any gain in capacitance per unit area otherwise achieved by
5 using HSG instead of a planar electrode. Use of other oxygen
6 containing high K dielectric materials has proved to create similar
7 problems.

8 Because it may be desirable to provide area enhancement of an
9 electrode in a MIM structure using HSG, one attempt at addressing the
10 stated problem is forming a silicon nitride insulative barrier layer over
11 the HSG. The silicon nitride barrier layer may be formed by nitridizing
12 the silicon of the outer surface of HSG. Unfortunately, silicon nitride
13 exhibits a K factor of only about 7, less than the K factor of some high
14 K factor dielectrics that are desirable. Accordingly, even the silicon
15 nitride barrier layer reduces the effective dielectric constant of the
16 capacitor.

17 SUMMARY OF THE INVENTION

18 In accordance with one aspect of the invention, a capacitor
19 fabrication method may include forming a first capacitor electrode over
20 a substrate and atomic layer depositing an insulative barrier layer to
21 oxygen diffusion over the first electrode. The method may further
22 include forming a capacitor dielectric layer over the first electrode and
23

1 forming a second capacitor electrode over the dielectric layer. By way
2 of example, the atomic layer deposited barrier layer may comprise Al_2O_3 .
3 Also, the barrier layer may exhibit a K factor of greater than about 7
4 at 20°C. The dielectric layer may be over the barrier layer.

5 In another aspect of the invention, a capacitor fabrication method
6 includes forming a first capacitor electrode over a substrate, chemisorbing
7 a layer of a first precursor at least one monolayer thick over the first
8 electrode, and chemisorbing a layer of a second precursor at least one
9 monolayer thick on the first precursor layer. A chemisorption product
10 of the first and second precursor layers may be comprised by a layer of
11 an insulative barrier material. A capacitor dielectric layer may be
12 formed over the first electrode and a second capacitor electrode may be
13 formed over the dielectric layer. As an example, the first precursor may
14 comprise H_2O and the second precursor may comprise trimethyl
15 aluminum. The dielectric layer may contact the barrier layer.

16 In yet another aspect of the invention, a capacitor fabrication
17 method includes forming an opening in an insulative layer over a
18 substrate and forming a layer of polysilicon in the opening. The
19 polysilicon layer may be converted to a first capacitor electrode. An
20 insulative barrier layer may be conformally formed on the first electrode
21 and may comprise Al_2O_3 . The barrier layer may be sufficiently thick and
22 dense to reduce oxidation of the first electrode by oxygen diffusion from
23 over the barrier layer. The method may further include forming a

1 capacitor dielectric layer comprising oxygen on the barrier layer and
2 forming a second capacitor electrode over the dielectric layer.

3 Other aspects of the invention include the capacitor constructions
4 formed from the above described methods.

5 6 BRIEF DESCRIPTION OF THE DRAWINGS

7 Preferred embodiments of the invention are described below with
8 reference to the following accompanying drawings.

9 Fig. 1 is an enlarged view of a section of a semiconductor wafer
10 at one processing step in accordance with the invention.

11 Fig. 2 is an enlarged view of the section of the Fig. 1 wafer at
12 a processing step subsequent to that depicted by Fig. 1.

13 Fig. 3 is an enlarged view of the section of the Fig. 1 wafer at
14 a processing step subsequent to that depicted by Fig. 2.

15 Fig. 4 is an enlarged view of the section of the Fig. 1 wafer at
16 a processing step subsequent to that depicted by Fig. 3.

17 Fig. 5 is an enlarged view of the section of the Fig. 1 wafer at
18 a processing step subsequent to that depicted by Fig. 4.

19 Fig. 6 is an enlarged view of the section of the Fig. 1 wafer at
20 a processing step subsequent to that depicted by Fig. 5.

21 Fig. 7 is an enlarged view of a section of an alternate embodiment
22 semiconductor wafer processed in accordance with alternate aspects of the
23 invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Atomic layer deposition (ALD) involves formation of successive atomic layers on a substrate. Such layers may comprise an epitaxial, polycrystalline, amorphous, etc. material. ALD may also be referred to as atomic layer epitaxy, atomic layer processing, etc. Further, the invention may encompass other deposition methods not traditionally referred to as ALD, for example, chemical vapor deposition (CVD), but nevertheless including the method steps described herein. The deposition methods herein may be described in the context of formation on a semiconductor wafer. However, the invention encompasses deposition on a variety of substrates besides semiconductor substrates.

In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

1 Described in summary, ALD includes exposing an initial substrate
2 to a first chemical species to accomplish chemisorption of the species
3 onto the substrate. Theoretically, the chemisorption forms a monolayer
4 that is uniformly one atom or molecule thick on the entire exposed
5 initial substrate. In other words, a saturated monolayer. Practically, as
6 further described below, chemisorption might not occur on all portions
7 of the substrate. Nevertheless, such an imperfect monolayer is still a
8 monolayer in the context of this document. In many applications, merely
9 a substantially saturated monolayer may be suitable. A substantially
10 saturated monolayer is one that will still yield a deposited layer
11 exhibiting the quality and/or properties desired for such layer.

12 The first species is purged from over the substrate and a second
13 chemical species is provided to chemisorb onto the first monolayer of the
14 first species. The second species is then purged and the steps are
15 repeated with exposure of the second species monolayer to the first
16 species. In some cases, the two monolayers may be of the same species.
17 Also, a third species or more may be successively chemisorbed and
18 purged just as described for the first and second species.

19 Purging may involve a variety of techniques including, but not
20 limited to, contacting the substrate and/or monolayer with a carrier gas
21 and/or lowering pressure to below the deposition pressure to reduce the
22 concentration of a species contacting the substrate and/or chemisorbed
23 species. Examples of carrier gases include N₂, Ar, He, Ne, Kr, Xe, etc.

1 Purging may instead include contacting the substrate and/or monolayer
2 with any substance that allows chemisorption byproducts to desorb and
3 reduces the concentration of a contacting species preparatory to
4 introducing another species. A suitable amount of purging can be
5 determined experimentally as known to those skilled in the art. Purging
6 time may be successively reduced to a purge time that yields an increase
7 in film growth rate. The increase in film growth rate might be an
8 indication of a change to a non-ALD process regime and may be used
9 to establish a purge time limit.

10 ALD is often described as a self-limiting process, in that a finite
11 number of sites exist on a substrate to which the first species may form
12 chemical bonds. The second species might only bond to the first species
13 and thus may also be self-limiting. Once all of the finite number of
14 sites on a substrate are bonded with a first species, the first species will
15 often not bond to other of the first species already bonded with the
16 substrate. However, process conditions can be varied in ALD to
17 promote such bonding and render ALD not self-limiting. Accordingly,
18 ALD may also encompass a species forming other than one monolayer
19 at a time by stacking of a species, forming a layer more than one atom
20 or molecule thick. The various aspects of the present invention
21 described herein are applicable to any circumstance where ALD may be
22 desired. Often, traditional ALD occurs within an often-used range of
23 temperature and pressure and according to established purging criteria

1 to achieve the desired formation of an overall ALD layer one monolayer
2 at a time. Even so, ALD conditions can vary greatly depending on the
3 particular precursors, layer composition, deposition equipment, and other
4 factors according to criteria known by those skilled in the art.
5 Maintaining the traditional conditions of temperature, pressure, and
6 purging minimizes unwanted reactions that may impact monolayer
7 formation and quality of the resulting overall ALD layer. Accordingly,
8 operating outside the traditional temperature and pressure ranges may
9 risk formation of defective monolayers.

10 The general technology of chemical vapor deposition (CVD)
11 includes a variety of more specific processes, including, but not limited
12 to, plasma enhanced CVD and others. CVD is commonly used to form
13 non-selectively a complete, deposited material on a substrate. One
14 characteristic of CVD is the simultaneous presence of multiple species
15 in the deposition chamber that react to form the deposited material.
16 Such condition is contrasted with the purging criteria for traditional ALD
17 wherein a substrate is contacted with a single deposition species that
18 chemisorbs to a substrate or previously deposited species. An ALD
19 process regime may provide a simultaneously contacted plurality of
20 species of a type or under conditions such that ALD chemisorption,
21 rather than CVD reaction occurs. Instead of reacting together, the
22 species may chemisorb to a substrate or previously deposited species,
23 providing a surface onto which subsequent species may next chemisorb

1 to form a complete layer of desired material. Under most CVD
2 conditions, deposition occurs largely independent of the composition or
3 surface properties of an underlying substrate. By contrast, chemisorption
4 rate in ALD might be influenced by the composition, crystalline
5 structure, and other properties of a substrate or chemisorbed species.
6 Other process conditions, for example, pressure and temperature, may
7 also influence chemisorption rate.

8 ALD, as well as other deposition methods and/or methods of
9 forming insulative barrier layers may be useful in capacitor fabrication
10 methods. According to one aspect of the invention, a capacitor
11 fabrication method includes forming a first capacitor electrode over a
12 substrate and atomic layer depositing an insulative barrier layer to oxygen
13 diffusion over the first electrode. A capacitor dielectric layer may be
14 formed over the first electrode and a second capacitor electrode may be
15 formed over the dielectric layer. At least one of the first or second
16 electrodes may comprise polysilicon, which may be rugged polysilicon,
17 preferably hemispherical grain (HSG) polysilicon. Also, at least one of
18 the electrodes might comprise RuO_x . The dielectric layer may comprise
19 oxygen. Exemplary materials for the dielectric layer include, but are not
20 limited to, Ta_2O_5 , barium strontium titanate, TiO_2 , Y_2O_3 , HfO_2 , ZrO_2 ,
21 HfSiO_2 , ZrSiO_2 , etc.

22 Notably, the insulative barrier layer to oxygen diffusion formed
23 over the first electrode may provide the advantage of reducing oxidation

1 of the electrode by oxygen diffusion from an oxygen source, for example,
2 the dielectric layer. The dielectric may be formed over the barrier layer,
3 thus, the barrier layer may reduce oxygen diffusion to the first capacitor
4 electrode. Alternatively, such barrier layer may reduce oxygen diffusion
5 from the first capacitor electrode or under the first capacitor electrode
6 to the dielectric layer or second capacitor electrode. It follows then that
7 the barrier layer may also be formed over the capacitor dielectric layer
8 with the second capacitor electrode over the barrier layer such that the
9 barrier layer reduces oxygen diffusion from the dielectric layer to the
10 second electrode. Such positioning may also reduce oxygen diffusion
11 from over the dielectric layer to the first capacitor electrode, for
12 example, oxygen diffusion from the second capacitor electrode. Such
13 may be a problem when the second capacitor electrode comprises RuO_x .

14 Accordingly, one aspect of the invention may include atomic layer
15 depositing the barrier layer over the first electrode, forming the dielectric
16 layer over the barrier layer, and atomic layer depositing another
17 conductive barrier layer to oxygen diffusion over the dielectric layer.
18 Forming the first and second electrodes and dielectric layer may be
19 accomplished by methods known to those skilled in the art and may
20 include atomic layer deposition, but preferably other methods.

21 The atomic layer depositing of the barrier layer may occur at a
22 temperature of from about 100 to about 600°C and at a pressure of
23 from about 100 milliTorr (mT) to about 10 Torr (T). The atomic layer

1 deposited barrier layer may exhibit a K factor of greater than about 7
2 at 20°C. Preferably, the barrier layer may exhibit a K factor of about
3 10 at 20°C. One particularly suitable material for the barrier layer
4 includes Al_2O_3 . The barrier layer may have a thickness of less than
5 about 30 Angstroms or another thickness depending on the material
6 properties. Preferably, the barrier layer may have a thickness of less
7 than about 12 Angstroms, or more preferably less than about 6
8 Angstroms. As an example, a 30 Angstrom film of Al_2O_3 protected a
9 WN film from oxidation during annealing at 700 °C for 60 seconds in
10 an O_2 ambient. Thinner Al_2O_3 films may also be suitable.

11 One consideration in selecting a material for the barrier layer is
12 the thickness and density of the barrier layer that will be sufficient to
13 achieve a desired level of oxygen diffusion reduction. Another factor to
14 evaluate is that the barrier layer might be considered to form a part of
15 a capacitor dielectric when the barrier layer contacts the dielectric layer
16 since the barrier layer is insulative. Accordingly, it may be advantageous
17 to recalculate the desired dimensions of a dielectric layer contacted by
18 the barrier layer accounting for the presence of the additional insulative
19 material. Accordingly, an "insulative" material as the term is used
20 herein designates a material exhibiting a conductivity at 20°C of less
21 than 10^4 microOhm⁻¹ centimeter⁻¹. As an alternative, an "insulative"
22 material in the present context might be viewed as a material that
23 impacts the capacitance otherwise achieved without the material.

1 Generally, a "conductive" or "semiconductive" material might not produce
2 a change in capacitance as such a barrier layer. A combined capacitor
3 dielectric and insulative barrier layer according to the aspects of the
4 invention can exhibit a leakage current of less than about 10^{-15} amps per
5 cell and yield a capacitance of greater than about 20 femtoFarads per
6 cell.

7 As another aspect of the invention, a capacitor fabrication method
8 may include forming a first capacitor electrode over a substrate,
9 chemisorbing a layer of a first precursor at least one monolayer thick
10 over the first electrode, and chemisorbing a layer of a second precursor
11 at least one monolayer thick over the first precursor layer. A
12 chemisorption product of the first and second precursor layers may be
13 comprised by a layer of an insulative barrier material. Because the
14 chemisorption product is comprised by the barrier layer, the barrier layer
15 may also include insulative barrier material that is not a chemisorption
16 product of the first and second precursor layers. A capacitor dielectric
17 layer may be formed over the first electrode and a second capacitor
18 electrode may be formed over the dielectric layer. The various positions
19 for the barrier layer discussed above are also applicable to the present
20 aspect of the invention.

21 In forming the chemisorption product of the first and second
22 precursor layers, the first and second precursor layers may each consist
23 essentially of a monolayer. Further, the first and second precursor layers

1 may each comprise substantially saturated monolayers. The extent of
2 saturation might not be complete and yet the barrier layer may
3 nevertheless provide the desired properties. Thus, substantially saturated
4 may be adequate. The first and second precursor may each consist
5 essentially of only one chemical species. However, as described above,
6 precursors may also comprise more than one chemical species.
7 Preferably, the first precursor is different from the second precursor,
8 although for some barrier layers, the first and second precursor might
9 be the same.

10 One example of a precursor pair for forming Al_2O_3 includes H_2O
11 and trimethyl aluminum (TMA). It is conceivable that more than one
12 pair of precursors may comprise the first and second precursors, but
13 preferably only one pair. Additional alternating first and second
14 precursor layers may be chemisorbed in keeping with the above aspect
15 of the invention to achieve a desired thickness for the barrier layer.

16 Although ALD and/or chemisorbing the first and second precursors
17 may be suitable for forming a barrier layer, other methods may also be
18 suitable. Accordingly, a variety of barrier layer forming techniques may
19 be used in combination with techniques to increase electrode surface area
20 to provide enhancement of capacitance per unit area. Figs. 1-6
21 exemplify the features of the various aspects of the invention described
22 above, as well as other aspects of the invention. For example, enhancing
23 capacitance per unit area.

Turning to Fig. 1, wafer portion 1 is shown including a substrate 2 with an insulative layer 4 formed thereon. A capacitor fabrication method may include forming an opening 16 in insulative layer 4, the opening 16 having sides and a bottom. Turning to Fig. 2, a layer of polysilicon 6 may be formed over the sides and bottom of the opening. Polysilicon layer 6 may then be converted to a first capacitor electrode 8 comprising hemispherical grain polysilicon, as shown in Fig. 3. In Fig. 4, an insulative barrier layer 10 may be conformally formed on first electrode 8. Barrier layer 10 may comprise Al_2O_3 and be sufficiently thick and dense to reduce oxidation of the first electrode by oxygen diffusion from over barrier layer 10. A capacitor dielectric layer 12 may be formed on barrier layer 10. One source of oxygen diffusion may be dielectric layer 12. In Fig. 5, a second capacitor electrode layer 14 is shown formed on dielectric layer 12. Fig. 6 shows excess portions of barrier layer 10, dielectric layer 12, and second capacitor electrode layer 14 removed from over insulative layer 4 to form a capacitor structure. As described above, a barrier layer may also be formed over a dielectric layer, thus Fig. 7 alternatively shows barrier layer 10 over dielectric layer 12.

As an example, Al_2O_3 deposition from TMA/ H_2O was conducted at a substrate temperature from about 300 to about 500 °C and chamber pressure of about 200 mT using a GENUS LYNX 2 (TM) ALD tool. The GENUS LYNX 2 (TM) tool controls gas flow rate using pressure

1 settings. The first step of the cycle included pulsing H_2O set at about
2 20-25 T for from about 200 to about 2000 microseconds (μsec) in a N_2
3 carrier set at about 40 T. A N_2 carrier set at about 74 T was pulsed
4 for from about 1 to about 3 sec to purge the H_2O . Next, TMA set at
5 about 20-25 T was pulsed for from about 80 to about 1000 μsec in a
6 N_2 carrier set at about 40 T followed by purging as indicated to
7 complete the cycle. Gases were removed using an exhaust pump. The
8 Al_2O_3 formed exhibited a K factor of approximately 9.

9 In compliance with the statute, the invention has been described
10 in language more or less specific as to structural and methodical
11 features. It is to be understood, however, that the invention is not
12 limited to the specific features shown and described, since the means
13 herein disclosed comprise preferred forms of putting the invention into
14 effect. The invention is, therefore, claimed in any of its forms or
15 modifications within the proper scope of the appended claims
16 appropriately interpreted in accordance with the doctrine of equivalents.
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